National Supercomputer Projects in Japan

Jun Makino
TiTech

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Talk Structure

- National Supercomputer Projects
- The “K” computer
- Post-petascale project

National Supercomputer Projects

- MITI
  - Super-high-performance computer (1966-75?)
  - High-speed computing system (1981-89)
  - Fifth generation (1982-91)
  - RWCP (1992-2001)
- MEXT
  - Numerical Wind Tunnel (?-1993)
  - CP-PACS (1992-96)
  - Earth Simulator (-2002)
  - The K Computer (2006-2012)

The level of success

High-speed computing system	**bad**
Fifth Generation	**bad**
RWCP	**bad**
NWT	**Very good**
CP-PACS	**Good**
ES	**fairly good**
K	**??**

NWT and CP-PACS have commercial offsprings: VPP500, SR-2201

Characteristics of failed and succeeded projects

- NWT, CP-PACS
  - Single science goal
  - Single person as the leader (Miyoshi, Iwasaki)
- Other projects
  - General Purpose
  - No single clear leader
  - Driven by politicians/bureaucrats

The case of K computer

It is certainly not a complete failure, but has numerous problems.
Rough time sequence

- **2004: Discussion started in the working group for computational science, committee for information science and technology, MEXT.**
- **2005: Interim report**
  - **Combines the requests from eight fields (at least formally)**
  - **Vector 2PF, Scalar parallel4PF, Accelerator 20PF**
- **2006: Design competition organized**

Time sequence continued

- **2005: Evaluation by CSTP (Council for Science and Technology) Target performance and many other details change**
- **Early 2006: Watanabe (from NEC) became the head of the project.**
- **Summer 2007: System architecture determined. Vector + Scalar**
- **Spring 2009: NEC (Vector) dropped out**
- **Oct 2010 Prototype machine appeared in Top 500**
- **June 2011Top 1**
- **Nov 2011 Keeps Top 1**

Problems with K project

- The target of the project was discussed in WG, but not clearly defined.
- Project started without clear single goal
- Performance target changed many times
- Architecture plan also changed several times
- One of the vendors dropped out (very exceptional in Japan)

Why this happened?

The WG discussion on the target

- This implies that the discussion was just to make up reasons to explain why the development of a supercomputer was important. The conclusion, its importance, was predetermined.
- In the case of NWT and CP-PACS, the target was clear right from the beginning
- Discussion in the WG resulted in: include all requests from all fields, but silently drop things which are difficult

Why this happened? (2)

Performance target changed many times

- Simply because the first performance target was way too low for the budget size
- The performance target was low because it was based on the predictions of vendors (so called "the three companies")
- The predictions of the vendors was low because their product line had become obsolete

In short,

Architecture design and development style are both wrong

Outcome: the vendor for vector processor dropped out in the middle of the five year development pe

Why the development style was wrong

- Probably because the planners wanted to follow the "success" in 70s and 80s
  - Supercomputers drives semiconductor development
  - With superior manufacturing technology, mak better product than US ones
- Reality
  - Smart phones drive semiconductor technology
  - Japanese semiconductor industry was about to vanish

Summary for K

- As the development project:
  - Too low goals
  - Even low goals were difficult or impossible to achieve due to outdated approach
- Basic reason: the (implicit) goal was to start a project to develop Japanese supercomputer, without the analysis of the if the outcome is useful/competitive.

Japanese Exascale Project

- Unfortunately, follows the path of the K computer
- WG (or three WGs....) formed in July 2011
- I am a member of "application WG"
- I proposed to map applications on the plane of B/F and total memory amount
- and proposed three concepts (beside "baseline")

1+3 architectures

Type	B/F	M/F
Baseline	0.1	0.01-0.1
System on Chip	4	10^{-5}
Accelerator	$10^{-3\sim2}$	0.001-0.01
Vector	1	1

What I hope

- Define clear single scientific goal for each architecture plan
- Assign single person as a leader, for at least SoC and accelerator projects