GRAPE-DR

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Talk structure

- GRAPE hardwares
  - GRAPE machines
  - GRAPE-DR

- How do they compare with GPGPU?

- GRAPE-DR project status
Short history of GRAPE

- Basic concept
- GRAPE-1 through 6
Basic concept

- With $N$-body simulation, almost all calculation goes to the calculation of particle-particle interaction.
- This is true even for schemes like Barnes-Hut treecode or FMM.
- A simple hardware which just calculates the particle-particle interaction can greatly accelerate overall calculation.
GRAPE-1 to GRAPE-6

GRAPE-1: 1989, 308Mflops
GRAPE-4: 1995, 1.08Tflops
GRAPE-6: 2002, 64Tflops
Processor LSI

- 0.25 µm design rule (Toshiba TC-240, 1.8M gates)
- 90 MHz Clock
- 6 pipeline processors
- 32.4 Gflops / chip
Performance history

Since 1995 (GRAPE-4), GRAPE has been faster than general-purpose computers.

Development cost was around 1/100.
Comparison with a recent Intel processor

<table>
<thead>
<tr>
<th></th>
<th>GRAPE-6</th>
<th>Intel Xeon 5365</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Year</strong></td>
<td>1999</td>
<td>2006</td>
</tr>
<tr>
<td><strong>Design rule</strong></td>
<td>250nm</td>
<td>65nm</td>
</tr>
<tr>
<td><strong>Clock</strong></td>
<td>90MHz</td>
<td>3GHz</td>
</tr>
<tr>
<td><strong>Peak speed</strong></td>
<td>32.4Gflops</td>
<td>48Gflops</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>10W</td>
<td>120 W</td>
</tr>
<tr>
<td><strong>Perf/W</strong></td>
<td>3.24Gflops</td>
<td>0.4 Gflops</td>
</tr>
</tbody>
</table>
“Problem” with GRAPE approach

- Chip development cost becomes too high.

<table>
<thead>
<tr>
<th>Year</th>
<th>Machine</th>
<th>Chip initial cost</th>
<th>process</th>
</tr>
</thead>
<tbody>
<tr>
<td>1992</td>
<td>GRAPE-4</td>
<td>200K$</td>
<td>1µm</td>
</tr>
<tr>
<td>1997</td>
<td>GRAPE-6</td>
<td>1M$</td>
<td>250nm</td>
</tr>
<tr>
<td>2004</td>
<td>GRAPE-DR</td>
<td>4M$</td>
<td>90nm</td>
</tr>
<tr>
<td>2008?</td>
<td>GDR2?</td>
<td>~ 10M$</td>
<td>65nm?</td>
</tr>
</tbody>
</table>

Initial cost should be 1/4 or less of the total budget. How we can continue?
Next-Generation GRAPE — GRAPE-DR

• Planned peak speed: 2 Pflops
• New architecture — wider application range than previous GRAPEs
• primarily to get funded
• No force pipeline. SIMD programmable processor
• Planned completion year: FY 2008 (early 2009)
Processor architecture

- Float Mult
- Float add/sub
- Integer ALU
- 32-word registers
- 256-word memory
- communication port
Chip structure

Collection of small processors.

512 processors on one chip
500MHz clock

Peak speed of one chip: 0.5 Tflops (20 times faster than GRAPE-6).
Why we changed the architecture?

• To get budget ($N$-body problem is too narrow...)
• To allow a wider range of applications
  – Molecular Dynamics
  – Boundary Element method
  – Dense matrix computation
  – SPH
• To allow a wider range of algorithms
  – FMM
  – Ahmad-Cohen
  – ...

Comparison with FPGA

- much better silicon usage (ALUs in custom circuit, no programmable switching network)
- (possibly) higher clock speed (no programmable switching network on chip)
- easier to program (no VHDL necessary; assembly language and compiler instead)
Comparison with GPGPU

Pros:

- Significantly better silicon usage (512PEs with 90nm)
- Designed for scientific applications reduction, small communication overhead, etc

Cons:

- Higher cost per silicon area... (small production quantity)
- Longer product cycle... 5 years vs 1 year

Good implementations of $N$-body code on GPGPU are coming (Hamada, Nitadori, Portegies Zwart, Harris, ...)
## Comparison with GPGPU(2)

<table>
<thead>
<tr>
<th></th>
<th>GRAPE-DR</th>
<th>nV G92</th>
<th>AMD</th>
<th>FS9170</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design rule</td>
<td>90</td>
<td>65</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td>Clock (GHz)</td>
<td>0.5</td>
<td>1.5</td>
<td>0.8</td>
<td></td>
</tr>
<tr>
<td># FPUs</td>
<td>512</td>
<td>112</td>
<td>320</td>
<td></td>
</tr>
<tr>
<td>SP peak (GF)</td>
<td>512</td>
<td>336</td>
<td>512</td>
<td></td>
</tr>
<tr>
<td>DP peak (GF)</td>
<td>256</td>
<td>—</td>
<td>?</td>
<td></td>
</tr>
<tr>
<td>Power (W)</td>
<td>65</td>
<td>70?</td>
<td>150?</td>
<td></td>
</tr>
</tbody>
</table>
How do you use it?

- **GRAPE**: The necessary software is now ready. Essentially the same as GRAPE-6.
- **Matrix etc ...**: RIKEN/NAOJ will do something
- **New applications:**
  - Primitive Compiler available
  - For high performance, you need to write the kernel code in assembly language (for now)
Primitive compiler
(Nakasato 2006)

/VARI  xi, yi, zi, e2;
/VARJ  xj, yj, zj, mj;
/VARF  fx, fy, fz;
dx = xi - xj;
dy = yi - yj;
dz = zi - zj;
r2 = dx*dx + dy*dy + dz*dz + e2;
r3i = powm32(r2);
ff = mj*r3i;
fx += ff*dx;
fy += ff*dy;
fz += ff*dz;

- Assembly code
- Interface/driver functions
- SIMD parallel data distribution
- Data reduction

are generated from this ”high-level description”.
(Can be ported to GPUs)
Interface functions

struct SING_hlt_struct0{
    double xi;
    double yi;
    double zi;
    double e2;
};

int SING_send_i_particle(struct SING_hlt_struct0 *ip, int n);
...

int SING_send_elt_data0(struct SING_elt_struct0 *ip, int index_in_EM);
...

int SING_get_result(struct SING_result_struct *rp);

int SING_grape_run(int n);
A few more words on software

- The right way to separate the task between host CPU and (GRAPE, GRAPE-DR, GPU, FPGA) is the same

- The right way to make efficient use of large number of processors on (GRAPE, GRAPE-DR, GPU, FPGA, CPU) is the same

We should develop a common software platform for different hardwares
Development status

Sample chip delivered May 2006
PE Layout

0.7mm by 0.7mm
Black: Local Memory
Red: Reg. File
Orange: FMUL
Green: FADD
Blue: IALU
• 32PEs in 16 groups
• 18mm by 18mm
Prototype board

2nd prototype. (Designed by Toshi Fukushige)

Single-chip board

PCI-Express x8 interface

On-board DRAM

Designed to run real applications

(Mass-production version will have 4 chips)
Preliminary data for first commercial version

- Prototype board working
- 1 Chip on a board (0.5Tflops peak)
- PCI-Express x4 interface
- 80W ...
- ∼ 5K USD ...
GDR-2?

- We are trying hard to “steal” some money from Japan’s “Next-Generation Supercomputer Project”

- With 65nm, it is not difficult to achieve
  - 768 DP Gflops/chip
  - 1.5 SP Tflops/chip
  - On-chip memory (16-32MB)
Summary

- GRAPE-DR, with programmable processors, will have wider application range than traditional GRAPEs.
- Production version board is now working.
- Commercial version should be ready by... sometime early next year
- Peak speed of a card with 4 chips will be 2 Tflops.